IN THE SPECIFICATION

Please amend the Specification as follows:

Paragraph beginning at Page 57, Line 2:

The MPU supports single-precision (32-bit) and double-precision (64-bit) IEEE floating-point math software. Rather than a floating-point unit and the silicon area it would require, the MPU contains instructions to perform most of the time-consuming operations required when programming basic floating-point math operations. Existing integer math operations are used to supply the core add, ~~substract~~ subtract, multiply and divide functions, while special instructions are used to efficiently manipulate the exponents and detect exception conditions. Additionally, a three-bit extension to the top one or two stack cells (depending on the precision) is used to aid in rounding and to supply the required precision and exception signaling operations.

Paragraph beginning at Page 79, Line 31:

An IOP program can be used to eliminate an extensive amount of external logic and ~~simply~~ simplify system designs. Further, by using the IOP 110 for timing-dependent system and application operations, timing constraints on the MPU program can often be eliminated or greatly relaxed.

Paragraph beginning at Page 94, Line 22:

The DMAC 112 can also be used to count events, and to interrupt the MPU 108 when a given count is reached. To do this, events are designed to produce a normal DMA memory read request, and the resulting transfer cycle increments the "address" in the corresponding global register. This "address" becomes the event counter. The MPU can also examine the register at any time to determine how many events have occurred. To interrupt the MPU after a given event count, program the global register for a negative count value within bits 9-2, and enable the page-boundary ~~interrup~~ interrupt. The MPU 108 will be interrupted when the counter reaches zero.